#5/B

OKON 1/11/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
Stephen M. Gates

Serial No.: 10/080,568

Group Art Unit: 2814

Filed: February 25, 2002

Examiner: P. Cao

For: FORMATION OF ARRAYS OF MICROELECTRONICS ELEMENTS

Honorable Commissioner of Patents
Washington, D.C. 20231

AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

In response to the Office Action dated October 2, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims to read as follows:

B1 Cont

11. (Amended) An array of microelectronic elements comprising:

a substrate of semiconductor material,

a lower layer of dielectric material disposed with a lower surface in contact with said substrate and an upper surface in spaced adjacency thereto,

a pattern of mutually electrically isolated metal conductors disposed within said lower layer of dielectric material, said metal conductors comprising a plurality of spaced apart conducting regions extending to said upper surface of said lower layer,

an upper layer of dielectric material disposed with a lower surface thereof in contact with and bonded to said upper surface of said lower layer, and

a plurality of nodes of semiconductor material disposed within said upper layer of dielectric material, each of said nodes being in electrical contact with only one of said conducting regions at said upper surface of said lower layer,

wherein each conducting region comprises a via comprising an electrically conducting material, each node being in electrical contact with said via.

12. (Amended) An array as set forth in claim 11, wherein each of said nodes comprises a